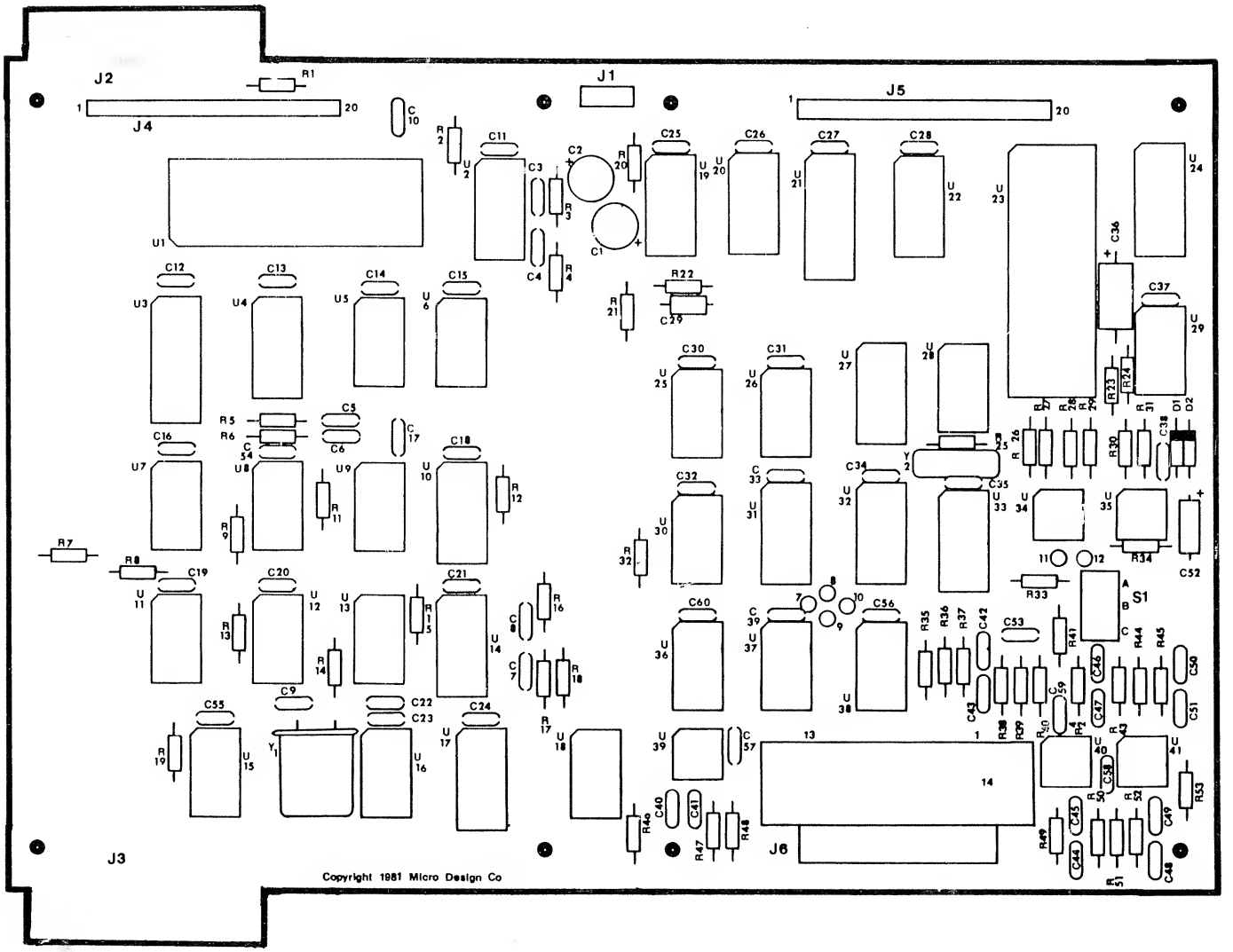
MDX-3

INTERFACE EXPANSION BOARD



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MDX-3
SYSTEM INTERFACE EXPANSION BOARD

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Revision 1.1

* TRS-80 is a trademark of Radio Shack, a Tandy Corp.

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WARNING WARNING

Before building the MDX-3, read this manual completly.

This manual assumes that you have already installed your floppy disk drive(s) and the required power supply.

****

1.Ø INTRODUCTION

The MDX-3 is an expansion board designed to interface directly to your TRS-8Ø Model lll computer. It will enhance the capabilities of your basic system to that beyond any other expansion board available. We at MD feel it is by far the BEST buy on the market. If you have any problems, please give MD a call.

1.1 HARDWARE FEATURES

- o Double Density Floppy Disk Controller
- o Serial Port (2Øma and RS232)
- o Direct Coupled Phone Modem (3ØØ Baud)

1.2 SOFTWARE FEATURES

- o Fully compatible with Model III software

2.0 Design Overview

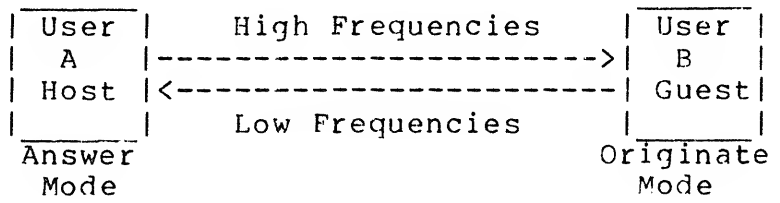
The MDX-3 is a bus extension to the TRS-80 Model III computer. It was designed to be a low cost, modular system. This modular design enables the user to assemble his board in the sequence he desires, at the time he desires. The basic sections are:

- o Floppy Disk Controller
- o Serial Interface
- o Phone Modem

The board mounts in the Model III at the location designated behind the processor board. Power is obtained from the CPU board power supply. The user must have a 16K level II system to operate the MDX-3.

2.1 Phone Modem

The phone modem is a 300 baud, direct connect modem. It uses a Frequency Shift Keying (FSK) modulation scheme. Two frequencies, 200 Hz apart, are used where a logic 1 (MARK) is the higher frequency and a logic 0 (SPACE) is the lower frequency. Two pairs of frequencies are used for simultaneous two-way communications,which is called "Full Duplex" operation. The lower pair is used for transmitting and the higher pair for receiving. A modem operating in this mode is called an "Originate Mode" device, since the terminal is usually used to originate the call to the computer. This mode may be used if the user is talking to a "host" computer set up to talk to a standard 300 baud terminal. It is also used by one of the two users (A and B) as per the example below (Fig 1). "Answer Mode" devices are just the opposite in that they transmit on the higher pair of frequencies and receive on the lower pair.



Dual Users Configuration

Fig. 1

Two TRS-80 users may communicate through the phone modem by designating one as the "host" (operates in the "answer mode"), and the other as the "guest" (operates in the "originate mode").

Since the phone modem is directly coupled to the phone line (i.e. no acoustic coupler is used), little or no noise will occur from outside interference. This results in very "quiet" modem operation.

This modem may also be used to communicate with both the Source* and Compu-Serve* as well as any other 300 baud machine.

2.2 Serial Interface

Serial interfacing is accomplished using a Western Digital TR1602B UART, a status buffer and a latch. The port can be configured for Data Terminal equipment (DTE) or Data Communications equipment (DCE) and is also baud rate selectable from 300 baud to 19200 baud (software programmable).

2.3 Floppy Disk Controller

The heart of the MDX-3 Floppy Disk Controller is the Western Digital FD1791B. This 40 pin I.C. takes care of most of the functions of FDC, including cyclic redundancy checks and all required logging of track location, sector location and I.D. field locations. Double-density operation is also a feature of the controller. Up to four floppy disk drives may be driven by the MDX-3. All TRS-80 compatible drives and all DOS software compatible with these drives will run with the MDX-3. * Source and Compu-Serve are trademarks of their respective companies.

3.Ø Parts List

The parts list is given in three sections:

1). Composite List
2). List By Sections
3). List By Numbers

The "composite list" is sorted by quantities of each part. This list is good for the user who plans to build the entire board. When all parts in the list are collected, the user is ready to assemble his board.

The "list by sections" should be used if the user plans to omit certain sections. This list gives the parts by sections. There are duplicates in this list where parts are used for more than one section.

The "list by numbers" should be used as a reference during trouble-shooting and when checking the locations of parts. It is sorted by device numbers.

There should be no substitutions to the parts list. 74ls parts must be used where called for. All 1% resistors MUST be the exact value called for . If parts called for in the parts list are used exclusively, trouble-free operation will result.

Parts List By Numbers

___	R1	150	OHM	1/4	W	5% RESISTOR
___	R2	1K	OHM	1/4	W	5% RESISTOR
___	R3	10K	OHM	1/4	W	5% RESISTOR
___	R4	27K	OHM	1/4	W	5% RESISTOR
___	R5	150	OHM	1/4	W	5% RESISTOR
___	R6	220	OHM	1/4	W	5% RESISTOR
___	R7	150	OHM	1/4	W	5% RESISTOR
___	R8	150	OHM	1/4	W	5% RESISTOR
___	R9	150	OHM	1/4	W	5% RESISTOR
___	R10	NOT USED				
___	R11	680	OHM	1/4	W	5% RESISTOR
___	R12	1K	OHM	1/4	W	5% RESISTOR
___	R13	10K	OHM	1/4	W	5% RESISTOR
___	R14	680	OHM	1/4	W	5% RESISTOR
___	R15	10K	OHM	1/4	W	5% RESISTOR
___	R16	270K	OHM	1/4	W	5% RESISTOR
___	R17	10K	OHM	1/4	W	5% RESISTOR
___	R18	150	OHM	1/4	W	5% RESISTOR
___	R19	1K	OHM	1/4	W	5% RESISTOR
___	R20	1K	OHM	1/4	W	5% RESISTOR
___	R21	1K	OHM	1/4	W	5% RESISTOR
___	R22	100	OHM	1/4	W	5% RESISTOR
___	R23	6.2K	OHM	1/4	W	5% RESISTOR
___	R24	4.7K	OHM	1/4	W	5% RESISTOR
___	R25	15M	OHM	1/4	W	5% RESISTOR
___	R26	100K	OHM	1/4	W	5% RESISTOR
___	R27	22K	OHM	1/4	W	5% RESISTOR
___	R28	600	OHM	1/4	W	5% RESISTOR
___	R29	22K	OHM	1/4	W	5% RESISTOR
___	R30	1K	OHM	1/4	W	5% RESISTOR
___	R31	2K	OHM	1/4	W	5% RESISTOR
___	R32	1K	OHM	1/4	W	5% RESISTOR
___	R33	100K	OHM	1/4	W	5% RESISTOR
___	R34	15K	OHM	1/4	W	5% RESISTOR
___	R35	680	OHM	1/4	W	5% RESISTOR
___	R36	1K	OHM	1/4	W	5% RESISTOR
___	R37	165K	OHM	1/4	W	1% RESISTOR
___	R38	845	OHM	1/4	W	1% RESISTOR
___	R39	21.5K	OHM	1/4	W	1% RESISTOR
___	R40	1.24K	OHM	1/4	W	1% RESISTOR
___	R41	1K	OHM	1/4	W	5% RESISTOR
___	R42	237K	OHM	1/4	W	1% RESISTOR
___	R43	8.87K	OHM	1/4	W	1% RESISTOR
___	R44	2.55K	OHM	1/4	W	1% RESISTOR
___	R45	97.6K	OHM	1/4	W	1% RESISTOR
___	R46	165K	OHM	1/4	W	1% RESISTOR
___	R47	267	OHM	1/4	W	1% RESISTOR
___	R48	18.7K	OHM	1/4	W	1% RESISTOR
___	R49	324	OHM	1/4	W	1% RESISTOR
___	R50	210K	OHM	1/4	W	1% RESISTOR
___	R51	8.66K	OHM	1/4	W	1% RESISTOR
___	R52	619	OHM	1/4	W	1% RESISTOR
___	R53	95.3K	OHM	1/4	W	1% RESISTOR

___	C1	22	UFD	ELEC. @16V CAP
___	C2	22	UFD	ELEC. @16V CAP
___	C3	51	PFD	@10V CAPACITOR
___	C4	.1	UFD	@16V CAPACITOR
___	C5	390	PFD	@10V CAPACITOR
___	C6	680	PFD	@10V CAPACITOR
___	C7	20	PFD	@10V CAPACITOR
___	C8	33	UFD	@10V CAPACITOR
___	C9	20	PFD	@10V CAPACITOR
___	C10	.01	UFD	@16V CAPACITOR
___	C11	.01	UFD	@16V CAPACITOR
___	C12	.01	UFD	@16V CAPACITOR
___	C13	.01	UFD	@16V CAPACITOR
___	C14	.01	UFD	@16V CAPACITOR
___	C15	.01	UFD	@16V CAPACITOR
___	C16	.01	UFD	@16V CAPACITOR
___	C17	.01	UFD	@16V CAPACITOR
___	C18	.01	UFD	@16V CAPACITOR
___	C19	.01	UFD	@16V CAPACITOR
___	C20	.01	UFD	@16V CAPACITOR
___	C21	.01	UFD	@16V CAPACITOR
___	C22	.01	UFD	@16V CAPACITOR
___	C23	.01	UFD	@16V CAPACITOR
___	C24	.01	UFD	@16V CAPACITOR
___	C25	.01	UFD	@16V CAPACITOR
___	C26	.01	UFD	@16V CAPACITOR
___	C27	.01	UFD	@16V CAPACITOR
___	C28	.01	UFD	@16V CAPACITOR
___	C29	100	PFD	@16V CAPACITOR
___	C30	.01	UFD	@16V CAPACITOR
___	C31	.01	UFD	@16V CAPACITOR
___	C32	.01	UFD	@16V CAPACITOR
___	C33	.01	UFD	@16V CAPACITOR
___	C34	.01	UFD	@16V CAPACITOR
___	C35	.01	UFD	@16V CAPACITOR
___	C36	25	UFD	ELEC. @16V CAP
___	C37	.01	UFD	@16V CAPACITOR
___	C38	.1	UFD	@16V CAPACITOR
___	C39	.01	UFD	@16V CAPACITOR
___	C40	.01	UFD	1% CAPACITOR
___	C41	.01	UFD	1% CAPACITOR
___	C42	.01	UFD	1% CAPACITOR
___	C43	.01	UFD	1% CAPACITOR
___	C44	.01	UFD	1% CAPACITOR
___	C45	.01	UFD	1% CAPACITOR
___	C46	.01	UFD	1% CAPACITOR
___	C47	.01	UFD	1% CAPACITOR
___	C48	.01	UFD	1% CAPACITOR
___	C49	.01	UFD	1% CAPACITOR
___	C50	.01	UFD	1% CAPACITOR
___	C51	.01	UFD	1% CAPACITOR
___	C52	10	UFD	ELEC. @16V CAP
___	C53	1	UFD	@16V CAPACITOR
___	C54	.01	UFD	@16V CAPACITOR
___	C55	.01	UFD	@16V CAPACITOR
___	C56	.01	UFD	@16V CAPACITOR
___	C57	1	UFD	@16V CAPACITOR
___	C58	1	UFD	@16V CAPACITOR
___	C59	1	UFD	@16V CAPACITOR
___	C60	.01	UFD	@16V CAPACITOR

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___ U1 WD1793
___ U2 74LS123
___ U3 74LS273
___ U4 74LS42
___ U5 74LS08
___ U6 74LS74
___ U7 7416
___ U8 7404
___ U9 74LS00
___ U10 74LS193
___ U11 7416
___ U12 74LS27
___ U13 74LS93
___ U14 74LS123
___ U15 74LS74
___ U16 7438
___ U17 74LS368
___ U18 7404
___ U19 74LS174
___ U20 74LS367
___ U21 74LS244
___ U22 74LS367
___ U23 WD1602 or equiv.
___ U24 BR1941 (Western Digital)
___ U25 7438
___ U26 7427
___ U27 74LS174
___ U28 MC1489 or equiv.
___ U29 7404
___ U30 74LS74
___ U31 74LS139
___ U32 74LS368
___ U33 MC14412
___ U34 MC1458 or equiv.
___ U35 MLM311 or equiv.
___ U36 MC1488 or equiv.
___ U37 MC1488 or equiv.
___ U38 MC1489 or equiv.
___ U39 MC1458 or equiv.
___ U40 MC1458 or equiv.
___ U41 MC1458 or equiv.

___ D1 1N4148
___ D2 IN4148

___ X1 16 MHZ CRYSTAL
___ X2 1 MHZ CRYSTAL

___ 5 8 PIN SOCKETS
___ 19 14 PIN SOCKETS
___ 12 16 PIN SOCKETS
___ 1 18 PIN SOCKETS
___ 2 20 PIN SOCKETS
___ 2 40 PIN SOCKETS

___ S1 3PDP PC MOUNT SWITCH

___ J4 20 PIN CONNECTOR
___ J5 20 PIN CONNECTOR
___ J6 DB-25 RIGHT-ANGLE CONNECTOR

___ MOUNTING HARDWARE (SUPPLIED W/BOARD)

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Composite Parts List

___	150 OHM 1/4W 5% RESISTOR	6	R1,R5,R7,R8,R9,R18
___	1K OHM 1/4W 5% RESISTOR	9	R2,R12,R19,R20,R21,R30,R32 R36,R41
___	10K OHM 1/4W 5% RESISTOR	4	R3,R13,R15,R17
___	27K OHM 1/4W 5% RESISTOR	1	R4
___	220 OHM 1/4W 5% RESISTOR	1	R6
___	680 OHM 1/4W 5% RESISTOR	3	R11,R14,R35
___	270K OHM 1/4W 5% RESISTOR	1	R16
___	100 OHM 1/4W 5% RESISTOR	1	R22
___	6.2K OHM 1/4W 5% RESISTOR	1	R23
___	4.7K OHM 1/4W 5% RESISTOR	1	R24
___	15M OHM 1/4W 5% RESISTOR	1	R25
___	100K OHM 1/4W 5% RESISTOR	2	R26,R33
___	22K OHM 1/4W 5% RESISTOR	2	R27,R29
___	600 OHM 1/4W 5% RESISTOR	1	R28
___	2K OHM 1/4W 5% RESISTOR	1	R31
___	15K OHM 1/4W 5% RESISTOR	1	R34
___	270K OHM 1/4W 5% RESISTOR	1	R16
___	165K OHM 1/4W 1% RESISTOR	1	R37
___	845 OHM 1/4W 1% RESISTOR	1	R38
___	21.5K OHM 1/4W 1% RESISTOR	1	R39
___	1.24K OHM 1/4W 1% RESISTOR	1	R40
___	237K OHM 1/4W 1% RESISTOR	1	R42
___	8.87K OHM 1/4W 1% RESISTOR	1	R43
___	2.55K OHM 1/4W 1% RESISTOR	1	R44
___	97.6K OHM 1/4W 1% RESISTOR	1	R45
___	165K OHM 1/4W 1% RESISTOR	1	R46
___	267 OHM 1/4W 1% RESISTOR	1	R47
___	18.7K OHM 1/4W 1% RESISTOR	1	R48
___	324 OHM 1/4W 1% RESISTOR	1	R49
___	210K OHM 1/4W 1% RESISTOR	1	R50
___	8.66K OHM 1/4W 1% RESISTOR	1	R51
___	619 OHM 1/4W 1% RESISTOR	1	R52
___	95.3K OHM 1/4W 1% RESISTOR	1	R53
___	22 UFD ELECTROLYTIC @16V	2	C1,C2
___	.1 UFD @16V	2	C4,C38
___	390 PFD @10V	1	C5
___	680 PFD @16V	1	C6
___	20 PFD @16V	2	C7,C9
___	51 PFD @10V	1	C3
___	33 UFD @10V	1	C8
___	.01 UFD @16V	30	C10-C28,C30-C35,C37,C39, C54,C55,C56
___	100 PFD @16V	1	C29
___	.01 UFD 1%	12	C40-C51

___	IN4148	2	D1,D2
___	16 MHZ CRYSTAL	1	X1
___	1 MHZ CRYSTAL	1	X2
___	8 PIN SOCKETS	5	
___	14 PIN SOCKETS	19	
___	16 PIN SOCKETS	12	
___	18 PIN SOCKETS	1	
___	20 PIN SOCKETS	2	
___	40 PIN SOCKETS	2	
___	3PDP PC MOUNT SWITCH	1	SW1
___	20 PIN CONNECTOR	2	J4,J5
___	DB-25 RIGHT-ANGLE CONNECTOR		
___	MOUNTING HARDWARE (SUPPLIED W/BOARD)		SUPPLIED
___	WD1793	1	U1
___	74LS123	2	U2,U14
___	74LS273	1	U3
___	74LS42	1	U4
___	74LS08	1	U5
___	74LS74	3	U6,U15,U30
___	7416	2	U7,U11
___	7404	3	U8,U18,U29
___	74LS00	1	U9
___	74LS193	1	U10
___	74LS27	1	U12
___	74LS93	1	U13
___	7438	2	U16,U25
___	74LS368	2	U17,U32
___	74LS174	2	U19,U27
___	74LS367	2	U20,U22
___	74LS244	1	U21
___	WD1602 or equiv.	1	U23
___	BR1941 (Western Digital)	1	U24
___	7427	1	U26
___	MC1489 or equiv.	2	U28,U38
___	74LS139	1	U31
___	MC14412	1	U33
___	MC1458 or equiv.	4	U34,U39-U41
___	MLM311 or equiv.	1	U35
___	MC1488 or equiv.	2	U36,U37

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FLOPPY DISK CONTROLLER

___ R1-R19
___ C1-C24,C54,C55
___ U1-U17
___ X1

SERIAL PORT

___ R21-R24,R32
___ C25,C33,C36,C37,C52
___ U18-U32,U36,U37,U38
___ X2
___ D1,D2

PHONE MODEM

The Phone Modem circuit requires the Serial Port logic.

___ R25-R31,R33-R53
___ C34,C35,C38-C51,C53,C56-C60
___ U28,U33,U34,U35,U37,39-U41

4.Ø Assembly

4.1 Overveiw

As stated before, the MDX-3 may be assembled in sections at the users discretion. Decide which sections you want to build and accumulate ALL parts required for that section before starting assembly. Use the "Composite Parts List" to find your parts, and use the "List By Numbers" to populate your board. Check off each component as you install it.

Before assembly begins, take a few minutes to visually inspect the PC board. Look for holes that didn't get drilled, good plate thru's, etc.This will keep debug time down to a minimum. If you follow the instructions closely, you will have no problems.

It is assumed that the user has a certain degree of knowledge of the tools necessary to build the board; i.e. the soldering iron and soldering techniques. Be very careful not to damage the traces or pads. They are VERY delicate. Excessive heat is unnecessary, and WILL damage them. Use a 25-3Ø watt iron for construction. DO NOT USE A SOLDER-GUN!!

You will need a pair of small dikes, a pair of long-nosed pliers, a screwdriver and a voltmeter.

It is imperative that sockets be installed for all I.C.'s. This will simplify troubleshooting and repair.

The step-by-step assembly instructions follow. Check off each step as it is completed. This will help you complete the assembly faster and more efficiently.

4.2 Assembly Instructions

____ Inspect your board for bad plate-thru's, bad solder-mask area's and general appearance.

____ Sort your parts into resistors, capacitors, sockets, ect.

____ Install all applicable I.C. sockets: starting in the upper left-hand corner, insert the appropriate size socket in the board. Be sure that you do not put a 16 pin socket in where a 14 pin socket belongs. This is easy to do were capacitors are positioned over device locations. Bend over the corner leads of the socket. This will hold it in place when you turn over the board. Repeat this proceedure for all sockets.

____ Turn the board over and solder all sockets in the board. Be careful not to cause solder bridges. Do not leave the soldering iron on too long as this may cause solder to flow thru the holes to the top side of the board and cause a short under the socket. A good solder connection should adhere to the lead.

____ Inspect board for cold solder joints and solder bridges.

____ Install all applicable resistors (see parts list): Starting with R1, check resistor for correct value, bend the leads with a pair of long-nose pliers to fit the appropriate holes, and insert the resistor in its place. Then bend the leads over so the part will stay in the board. Mark off R1 in the "Parts List By Numbers". Repeat this proceedure for 5 to 10 resistors. Recheck the resistors for correct value.

____ Turn the board over and solder these resistors in. Snip off the leads as close to the pads as possible. Repeat these last two steps until all resistors are installed.

____ Install all applicable capacitors (see parts list). Starting with C1, check the capacitor for correct value, bend the leads with a pair of long-nose pliers to fit the appropriate holes, and insert the capacitor in its place (WATCH POLARITIES where applicable). Then bend the leads over so the part will stay in the board. Mark off C1 in the "Parts List By Numbers". Repeat this proceedure for 5 to 10 capacitors. Recheck the capacitors for correct value and position.

____ Turn the board over and solder these capacitors in. Snip off the leads as close to the pads as possible. Repeat these last two steps until all capacitors are installed.

____ Install crystal X1 and X2. Solder the leads on the back of the board. Snip off excess leads.

____ Install diodes D1, and D2. NOTE POLARITIES. The little white band on one end of the diode distinguishes the polarity. The lead closest to this ring should be inserted in the hole indicated by the white stripe on the silk-screen. Insert D1 in its place and bend the leads to hold it in the board. Then invert the board, solder the leads and snip off the excess leads. Repeat for D2.

____ Install connectors J4 and J5. Solder them in place.

____ DO NOT INSTALL ANY JUMPERS OR I.C.'s AT THIS TIME!!!

5.Ø System Initialization

The following section assumes that the user has installed all sockets, resistors, capacitors, and all hardware required for the options selected. (NO I.C.'s).

If the sequence described below is followed, system initialization will be quick and easy.

5.1 Opening the Model III

The moment of truth draws near. We have come to the point were we must dare the unknown. You are ready to open your Model III computer.

Before breaking the Tandy installed seals, verify that all functions of your computer are working. This should include a check of the line printer, memory ("PRINT MEM") and user added modifications. Also keep in mind that you must always unplug the Model III (as apposed to only switching it off) before doing any work on the unit. This is because the power supplies still have one leg of power on them with the switch off.

If your system does not already have 48K of memory, you should strongly consider adding it at this time.

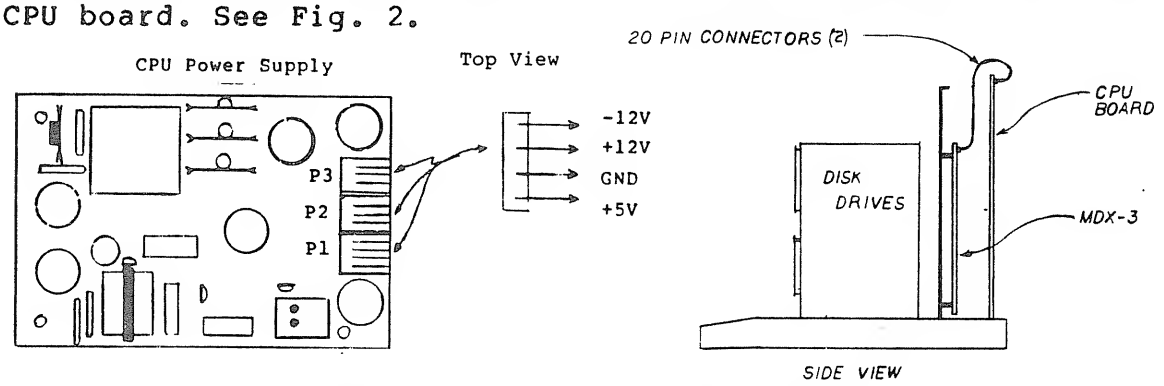
Lets begin. First, lay the computer on it's back and remove the 1Ø screws from the bottom of the Model III case. Be sure to keep track of were each screw came from as there are 3 diffrent sizes. Label them and place them in a container for safe storage.

Now upright your computer and remove the screw from the top back panel (does not apply to all models). VERY CAREFULLY lift the top cover straight up and away from the computer. Once you have cleared the computer base section, lay the top cover next to the computer right-side up. Move it as far away as possible to prevent damage. You are now ready to connect your MDX-3.

5.2 Connecting To The Model III

Three gore poly flat ribbon cables are required for the interface, one 2Ø pin for the serial port, one 2Ø pin for the FDC circuit and an 8 conductor cable for the CPU board (more later). These cables are available through our dealers (see list at end of manual). If you have built only the FDC or only the Serial Port and modem (either or) you need only install the appropriate connectors (J4 and the 1Ø conductor on the CPU for the FDC or J5 for the Serial Port).

First, insert the cable into the MDX-3 board. Making sure that you have pin 1 of the MDX-3 connected to pin 1 of the CPU board, push in the other side of the connector to the CPU board. See Fig. 2.

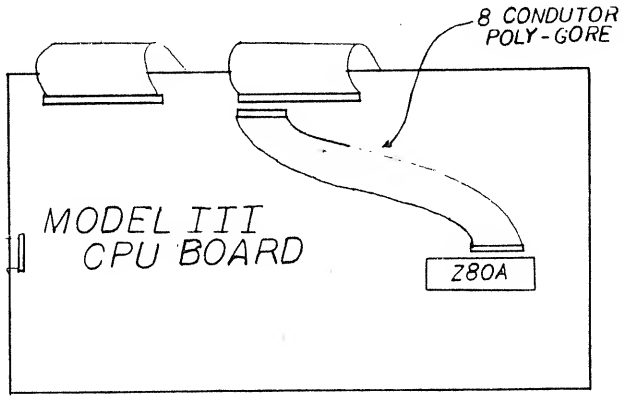


Connection To The MDX-3 Board

Fig. 2

Next, connect power to the board. You should have an extra tap on your power supply that drives the CPU board. Use this tap to power the MDX-3. Remember, +5, +12, and -12 volts are required to power the MDX-3. The power connections to the MDX-3 are labeled. BE SURE YOU CONNECT POWER CORRECTLY. See Fig. 2.

Install the 8 conductor cable in the two jumper plugs in the CPU board. See Fig. 3 for their locations. CAUTION: these poly cables are very fragile and can easily be broken internally. Take care when handling them and inserting them in their connectors.



Jumper Connection On The CPU Board

Fig. 3

5.3 System Power-Up

Do not install the MDX-3 in your computer until you are sure that it works. It is impossible to work on in the case! Set up a stand behind the computer to lay the MDX-3 on. This will allow easy access to the board. Place the monitor next to the keyboard.

There should be no I.C.'s installed yet.

Apply power to the MDX-3 by powering up your computer. Check immediatly for the three voltages. If they are not present, POWER DOWN. Check for solder bridges.

When you have all 3 voltages present, power down and install all applicatable components. Take care to install the IC's in the correct place and with pin 1 in the correct position (upper left corner of socket).

Now, apply power again and check for the appropriate voltages. If they are not present POWER DOWN. Check for parts inserted wrong.

When you have all parts installed and all voltages present, proceed to the next section.

5.4 Serial Port Test

The serial port is tested by looping the output data from the UART back to the input pin. Install a jumper wire from jumper 14 to jumper 16. Load a serial driver program and run it, (There is one in the Radio Shack Disk Operating Manual).

Now, anything typed on the keyboard should appear on the screen. If it does not, you have problems in your serial port circuitry. Refer to the trouble shooting section 7.2.

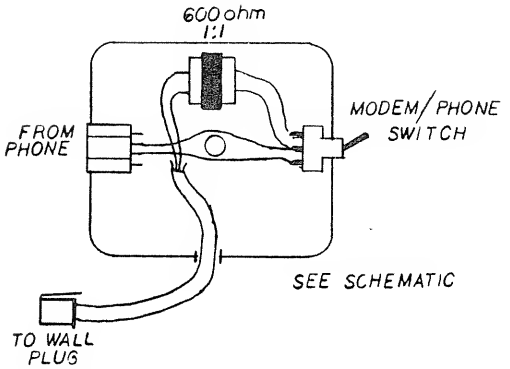
5.5 Phone Modem Test

The phone modem is tested using the Serial Port. For this reason, the Serial Port must have already been tested.

You must also build the circuit described in Fig. 4. It consist of a 600 ohm 1:1 transformer and a 3PDT switch. This circuitry is used to couple to the phone line.

We suggest that you buy a wall jack (available from your local Radio Shack store part # 279-355) and mount the transformer and switch inside of it. You can mount this contraption on the side of your computer for easy access to the Phone/Modem switch.

The MDX-3 Interface Board



Phone Modem Transformer Construction

Fig. 4

The MDX-3 board has provision for a PC mount switch to select between "answer" and "originate" modes. If you plan on switching modes, you may consider mounting this switch outside of the case for easy access. If you don't plan on changing modes, you may consider hard-wiring the mode you want.

The easiest way to check the phone modem is to attempt to connect over the phone line to another computer. To do this, jumper the modem to the Serial Port by connecting jumper 14 to jumper 15 and jumper 16 to jumper 17. Execute the communications program. Now dial up the "host" computer. When a tone is heard, switch the Phone/Modem switch to modem. This should connect you to the computer. You should now be able to log-on and communicate to the "Host" computer. If you have problems, try the method described below.

Jumper the modem to the Serial Port by connecting jumper 14 to jumper 15 and jumper 16 to jumper 17 . Then remove U33 (with power off) and bend up pins 2 and 10. Replace U33. Tie pin 2 to 5 volts and pin 10 to ground. This will put the 14412 Modem chip in the test mode. Power up the system and re-load the serial driver program. After initializing the program, any character typed will appear on the screen. After the phone modem has been deemed good, disconnect pins 2 and 10 of U33 and bend them back down. Replace U33. If you have problems, refer to the trouble-shoot section (section 7.3).

5.6 Floppy Disk Controller Test

Connect a drive cable from connector J2 of the MDX-3 to the floppy drive(s), making sure that pin 1 of your floppy disk drive connects to pin 1 of J2. Install a groung wire from the top of the CPU chassis to each drive.

Insert a system disk (write protected... i.e. write protection tab covered).Power up the Model lll. The drive should be selected and the motor activated. After a second, the DOS prompt should appear on the screen (this will vary between different DOS programs. See your DOS manual for details). To test the write capabilities, make a back-up copy of a DOS system diskette. Once again, see your DOS manual for further details. If you have problems, consult the troubleshooting section 7.1.

5.7 Installing The MDX-3

Now that you have proven your board 1ØØ% functional, you can install it in your computer.

Power down and unplug the computer. Remove the following cables from the CPU board:

1. Power connectors (upper right-hand corner)

2. The keyboard cable (left-hand side of board)

3. The cassette port connector (located just below the keyboard connector)

4. RS232 connectors (near power connectors)

5. The 2 flat ribbon cables from the CPU to the MDX-3

Remove the small bracket at the top of the board near the RS232 connector. It is held in by 2 screws and may have a ground strap attached.

Remove the screws that hold the CPU board in its frame. Now, carefully remove the CPU board by pressing the small tabs on the plastic spacer mounts that protrude through the PC board, and gently pull the PC board away from the frame. BE CAREFUL NOT TO LOOSE THE SPACERS that go between the PC board and the metal frame. They are used to isolate the backside of the board from the metal.

You will see 8 mounting holes in the frame for mounting the MDX-3. Some of them may be square. Mount 8 1/4" PLASTC stand-offs using 6/32 screws. Washers are needed on the square holes to prevent the screws from pulling thru the chassis.

With the component side of the MDX-3 facing you, insert the screws in the upper left and upper right-hand corners and screw them into the appropriete stand-offs. Now install the remaining 6 screws that hold the MDX-3 in place.

Remount the CPU board in the chassis. BE SURE THAT THE STANDOFFS ARE IN PLACE. Install the mounting screws.

Reconnect the cables to the CPU board as they were. BE sure to reconnect exactly as they were before.

When you have completed the instalaton of your drives, you are ready to re-test the system.

Retest the floppy disk controller again as described in section 5.6. Also test the serial port and phone modem again as described in sectios 5.4 and 5.5 respectfully.

If your system boots up and checks out good, you can now put the cover back on the computer. When doing this be VERY CAREFUL NOT TO DAMAGE THE YOKE OF THE PICTURE TUBE BY BUMPING IT ON THE CPU FRAME. When the cover is back in it's place and all wires are tucked into the case, you can invert the computer and install the cover screws.

6.Ø Circuit Description

This section has been written as an aid in trouble-shooting the board and enabling the user to better understand the product. The schematic should be used to follow the descriptions.

6.1 Serial Interface

To understand the workings of the MDX-3 Serial Interface, you will need to refer to the schematic and port configuration tables. For more information, refer to the TR16Ø2B data sheet in the appendix.

The RS-232 option supports synchronous serial transmissions and conforms to EIA RS-232 standards. The heart of the system is the Western Digital TR16Ø2B UART. This chip converts the parallel data from the CPU to serial data (including start, stop and parity bits), and vise-versa.

6.1.1 BAUD RATE GENERATOR

The transmit and receive clock rates that the TR16Ø2 require are generated by the BR1941 Baud Rate Generator. This device uses the 5.Ø688 MHZ clock provided by the CPU board and information from the CPU, and divides the basic clock into separate clocks, one for transmit and one for receive. These two signals provide the WD16Ø2 with the clock rates required. All rates are SETCOM compatable. See Fig. 5 for details.

Nibble Loaded	Baud Rate	16X Clock Frequency (KHZ)
ØH	5Ø	Ø.8
1H	75	1.2
2H	11Ø	1.76
3H	134.5	2.1523
4H	15Ø	2.4
5H	3ØØ	4.8
6H	6ØØ	9.6
7H	12ØØ	19.2
8H	18ØØ	28.8
9H	2ØØØ	32.Ø81
AH	24ØØ	38.4
BH	36ØØ	57.6
CH	48ØØ	76.8
DH	72ØØ	115.2
EH	96ØØ	113.6
FH	19,2ØØ	316.8

Baud Rate Frequencies

Fig. 5

6.1.2 PORT CONFIGUATION

The RS232 circuit is port mapped. Writing to or reading from the appropriate port will cause the corresponding function to execute. See Fig. 6 for a description of each port.

Port	Input	Output
E8	Modem Status	Master reset, enables UART control register load
E9	Toggles UART control register load	Baud rate register load enable bit
EA	UART Status	Uart control register load and Modem control
EB	Receiver Holding register	Transmitter Holding register

Ports Descriptions

Fig. 6

6.1.2.1 Port E8H

An output to this port causes a master reset to the UART and enables the control register load enable bit.

An input from port E8H is described in Fig. 7.

DATA BIT	FUNCTION
DØ	RECEIVER INPUT; UART PIN 2Ø DB-25
D1	UART CONTROL REG. LOAD STATUS; 1=ENABLED
D2	NOT USED
D3	NOT USED
D4	RING INDICATOR; PIN 22 DB-25
D5	CARRIER DETECT; PIN 8 DB-25
D6	DATA SET READY; PIN 6 DB-25
D7	CLEAR TO SEND; PIN5 DB-25

Port E8H Bit Definitions

Fig. 7

6.1.2.2 Port E9H

An output to this register loads the baud rate generator with a bite of code which determines the transmit and receive rate of the UART. The low order nibble determines the recieve rate and the high order nibble determines the transmit rate.

An input to this port toggles the UART control register enable bit.

6.1.2.3 Port EAH

The output function of this port is dependent upon the status of the UART Control Register Load Status bit (D1 port E8H). If this bit is a "1", then an output to port EAH will load the UART control register. This control register is five bits wide (D3-D7), leaving three bits for modem contol (DØ-D2). Three more modem bits were added by allowing software to enable or disable the UART Control register. The tables in Fig. 8 sumarrize the bit allowcations with the UART Control register enabled and disabled.

PORT EAH OUTPUT BITS WITH UART CONTROL REGISTER ENABLED

DATA BIT	FUNCTION
DØ	REQUEST TO SEND; PIN 4 DB-25
D1	DATA TERMINAL READY; PIN 2Ø DB-25
D2	BREAK; Ø=DISABLE TRANSMIT DATA (CONTINOUS SPACE)
D3	PARITY INHIBIT; 1=DISABLE PARITY
D4	STOP BIT SELECT; 1=TWO, Ø=ONE STOP BITS
D5	WORD LENGTH SELECT 2
D6	WORD LENGTH SELECT 1
D7	EVEN PARITY ENABLE

PORT EAH OUTPUT WITH UART CONTROL REGISTER DISABLED

DATA BIT	FUNCTION
DØ	REQUEST TO SEND; PIN4 DB-25
D1	DATA TERMINAL READY; PIN 2Ø DB-25
D2	BREAK; Ø=DISABLE TRANSMIT DATA
D3	PARITY ERROR; 1=CONDITION TRUE
D4	SECONDARY TRANSMIT DATA; PIN 14 DB-25
D5	SECONDARY UNASSIGNED; PIN 18 DB-25
D6	NOT USED
D7	NOT USED

PORT EAH INPUT BITS

DATA BIT	FUNCTION
DØ	NOT USED
D1	NOT USED
D2	NOT USED
D3	PARITY ERROR; 1=CONDITION TRUE
D4	FRAMING ERROR; 1=CONDITION TRUE
D5	OVERRUN ERROR; 1=CONDITION TRUE
D6	TRANSMIT HOLDING REGISTER EMPTY; 1= CONDITION T
D7	DATA RECIEVED; 1=CONDITION TRUE

UART Control Register Bit Definitons

Fig. 8

6.1.2.4 Port EBH

An output to this port loads the UART Transmit Holding Register with the word to be transmitted. This register should never be loaded until the Transmitter Holding Register Empty Bit (port EAH) is true.

An input from this port reads the UART Receive Data Holding Register. This register should not be read unless the Data Recieve Bit (port EAH) is true.

6.2 PHONE MODEM

Digital transmission uses a Frequency Shift Keying (FSK) modulation scheme. Two frequencies 200 hz apart are used where a logic 1 (mark) is the higher frequency and a logic 0 (space) is the lower frequency of the pair. Two pairs of these frequencies are used for two way communications. This is called Full Duplex operation and is usually limited to 300 baud. The lower pair of frequencies is used for transmission by a terminal while the higher pair is used for receiving. A modem operating in this mode is called an "originate mode" device since a terminal is usually used to originate the call to the computer. "Answer mode" devices operate in just the opposite manner (See Fig. 9).

	ORIGINATE	ANSWER
MARK	1270	2225
SPACE	1070	2025

Modem Operating Frequencies

Fig. 9

A 1 MHZ crystal provides a stable frequency reference. Pin U33-10 controls the mode of operation; a logic 1 is the "originate mode" and a logic 0 on this pin gives the "answer mode". The transmit data output is buffered by U34 and then mixed with the telephone input by U34-5&6. The purpose of this duplexer is to cancel out the transmit signal to the filter while amplifying the received signal. U39,U40 and U41 and the accompanying resistors and capacitors are 2 three stage filters used to further amplify the signals and reject noise and harmonics. The modem is designed to match the telephone lines 600 ohm impedence by connecting a 1:1 transformer. CONTACT YOUR LOCAL PHONE COMPANY FOR IMFORMATION ABOUT THIS CONNECTION. The output of the 14412 modem chip is jumpered to the serial port for operation by the MDX-3.

6.3 Floppy Disk Controller

The MDX-3 Floppy Disk Controller circuit supports both single and double-density encoding schemes. This allows the use of the "CONVERT" command to convert Model I software to run on the Model III computer. The double- density scheme allows for 1.8 times as much data to be stored on the Model III disk as opposed to the single-density Model I. Write precompensation is software programable starting at any track (although software automatically starts the precompensaton at tracks beyond 21). The MDX-3 will control up to 4 drives, with generally 2 drives being internal and two drives external. The system will also support double-headed drives allowing the storage capacity of four disk drives (8 if 80 track drives are used) to be contained inside the Model III case!!!

Data transfers are accomplished by CPU data requests. In double-density operation, data transfers from the FDC to the CPU are syncronized by forcing a wait to the CPU and then clearing the wait by a data request from the FDC chip.The end of data transfer is signaled by an NMI from the FDC chip. A "watch-dog" timer insures against any condition that may hang the wait line to the CPU for a period long enough to allow RAM to loose its contents.

6.3.1 Data Control

Data transfers are controlled by a combination of control signals "DISKIN", "DISKOUT" and "REG". "DISKIN" AND "DISKOUT" are tied directly to the 1793 to control data to and from the CPU.

The disk controller is a port mapped device. The ports are E4H,F0H,F1H,F2H,F3H and F4H. These ports are decoded by the CPU board.

6.3.2 NMI Logic

U15 latches data bits D6 and D7 on the rising edge of REG. The outputs of these latches generate non-maskable interrupts to the CPU. The interrupt conditions are programmed by writing to port E4H with the appropriate bits set. If data bit D7 is set, an interrupt is generated by the FDC. If D7 is reset, interrupts from the FDC are disabled. If D6 is set, an NMI will be generated by a FDC request. If D6 is reset, interrupts on FDC request are disable. A read from port E4H questions the disk controller board to determine the source of the NMI. D7 indicates the status of the FDC interrupt request (0=TRUE, 1=FALSE). D6 indicates the status of the front panel reset button. These status signals are gated to the CPU by REG.

6.3.3 Drive Select Logic

A write to port F4H selects the desired drive. The table below shows the corresponding bits.

D0 Selects drive 0 when set
D1 selects drive 1 when set
D2 selects drive 2 when set
D3 selects drive 3 when set
D4 selects side o when reset
selects side 1 when set
D5 write precomp. enabled when set
D6 generates WAIT if set
D7 selects double-density when set

U3 selects the drives, side and determines single or double-density (MFM/FM) when clocked by the falling edge of DRVSEL. The motor-on signal is generated by U14 by the rising edge of DRVSEL. The duration of the motor-on signal is developed by the RC time constant as a part of U14 and results in in the drive motor being turned on for about 3 seconds after a drive select has occured.

6.3.4 Wait State and Wait Time-out Logic

As previously stated, a WAIT to the CPU can be generated by a write to port F4H with D6 set. This causes pin 9 of U15 to go high and, unless there is a drive selected, this signal is inverted by U16 and sent to the CPU as an NMI where it forces the Z80A into a wait state. The Z80A will remain in this state until the wait signal is brought high again. Three input signals (IRQ,DRQ and MR) are fed to NOR gate U12 which, when set, clears the wait state to the CPU. U2 serves as a "watch-dog" timer to ensure that the contents of RAM are not lost (dynamic refreshes are disabled during CPU wait states). The "watch-dog" period is determined by the RC time constant of R4 and C4.

6.3.5 Clock Generation Logic

A 16MHZ crystal and 3 inverters generate a 16MHZ square-wave that is then divided down to 1 MHZ by a 4 bit divide-by- 2 counter. This 1MHZ clock is fed directly to the FDC chip to support its clock requirements. This 4 bit counter (U13) also provides the required clock signal used by the data recovery circuitry (U10 and U16) to derive the read clock (RCLK) signal from the raw data sent by the disk drives.

6.3.6 Write Precompensation Logic

The write precompensation logic is primarily comprised of a BCD to Decimal decoder (U4). When in the double-density mode, the signals EARLY and LATE are used to select the phase input (Ø1-Ø4) on the leading edge of WDIN. The double-density mode is determine by reading D7 which has been latched into U3. When WG is high, a write operation is in progress.

6.3.7 FDC Chip

The Western Digital WD1793 is a VLSI MOS device which performs the functions of a floppy disk controller/formatter in a single chip implementation. The following port addresses are assigned to the internal registers of the 1793.

PORT	FUNCTION
FØH	command/staus register
FlH	track register
F2H	Sector register
F3H	data register

7.Ø Troubleshooting

This section gives solutons to a few common problems found when checking the MDX-3 board. If you have tried all listed troubleshooting items given below, and your system still does not work, call Micro-Design for assistance.

7.1 Floppy Disk Controller

If you get no responce from your disk drives after attempting to boot-up:

1. Are you sure your DOS is good? Remember, you are running a double-density system. Your DOS should be a double-density DOS. If possible, try it in another system.

2. If your drives seem to work intermittently, try adding ground wires from the power supply to the MDX-3 and disk drives.

3. If your system displays "CASS?" after depressing the reset button, the problem may be in the 2Ø pin or 8 in jumper cables. Recheck them.

4. As stated before, some CPU boards just don't like to work with any controller boards. We have found that some type "F" boards require the changing of the Z8Ø to a Z8ØA to solve this problem.

5. Check the power supplies for proper voltages. You may have lost one along the way.

6. Check the configuration of your drives. See the owners manual for assistance.

7. Refer to the Circuit Description and schematic to troubleshoot.

7.2 Serial Port

If your serial port does not come up as described in section 5.4, then:

1. Recheck components for correct types and be sure all are installed correctly.

2. Check jumper configurations. In the test mode you should have JP-8 and JP-9 tied together. When you have finished with the test mode you must tie JP-8 to JP-10 and JP-9 to JP-7 to use the Phone Modem.

3. Check -12 volts with voltmeter.

4. Refer to the Circuit Description and schematic to troubleshoot.

7.3 Phone Modem

If your serial port test is good, but the phone modem does not work:

1. Check components for correct values. Remember, the 1% resistors and capacitors should be 1%.

2. Be sure all IC's are in the correct place and not upside-down.

3. If you experience noisy operation, try increasing R28 to 610 ohms.

4. Check jumpers for correct configuration. JP-8 to JP-10 and JP-7 to JP-9.

5. If you have another phone on the extension you are using for the modem link, set the Phone/Modem switch in the "Modem" position and listen on the other extension. You should hear a steady tone. When a key is depressed on the keyboard, you should hear a short change in the tone. This is the data going out from your computer. This test will help you to determine if you are sending data out.

8.Ø Conclusion

You have finally reached the end of this manual. Hopefully (!) you now have a working board that will bring you many hours of enjoyment and enable you to do the things that you anticipated when you entered into this venture. If at any time you have any problems, suggestions, comments or just want to rap, give us a call. We are very interested in your views. We have entered your name on our mailing list (unless otherwise requested) and will be sending you all updates, new modifications and any other material that may be beneficial to you..... So fire it up and ENJOY YOUR MDX-3!!!!!

9.0 APPENDIX

WESTERN DIGITAL
CORPORATION

FD 179X-02 Floppy Disk Formatter/Controller Family

MAY 1980

FEATURES

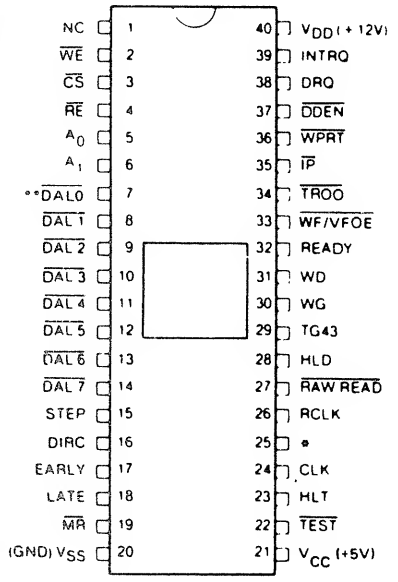
- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable length Sector
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

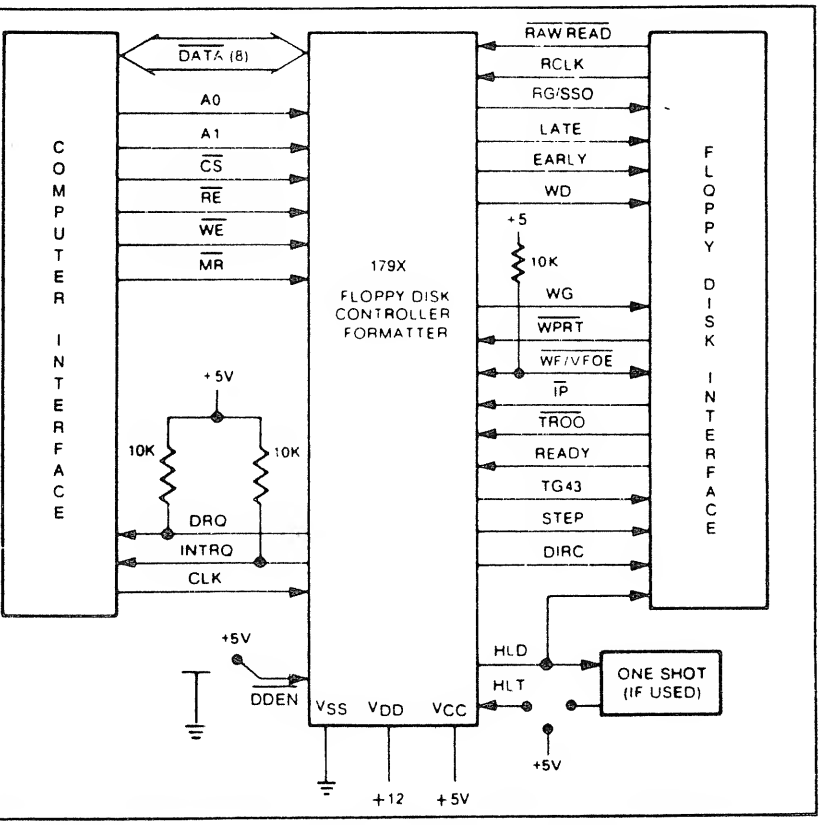
APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/ FORMATTER
NEW MINI-FLOPPY CONTROLLER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS

PIN CONNECTIONS



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{\text{MR}}$ ACTIVE. When $\overline{\text{MR}}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low.
3	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	A logic low on this input selects the chip and enables computer communication with the device.
4	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{\text{CS}}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control: A1 A0 $\overline{\text{RE}}$ $\overline{\text{WE}}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0}}$-$\overline{\text{DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{\text{WE}}$ or transmitter enabled by $\overline{\text{RE}}$.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE *(1791/3)*	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ / $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF}}$/$\overline{\text{VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

C O R P O R A T I O N

TR1602/TR1402/TR1863/TR1865
Universal Asynchronous Receiver/Transmitter (UART)

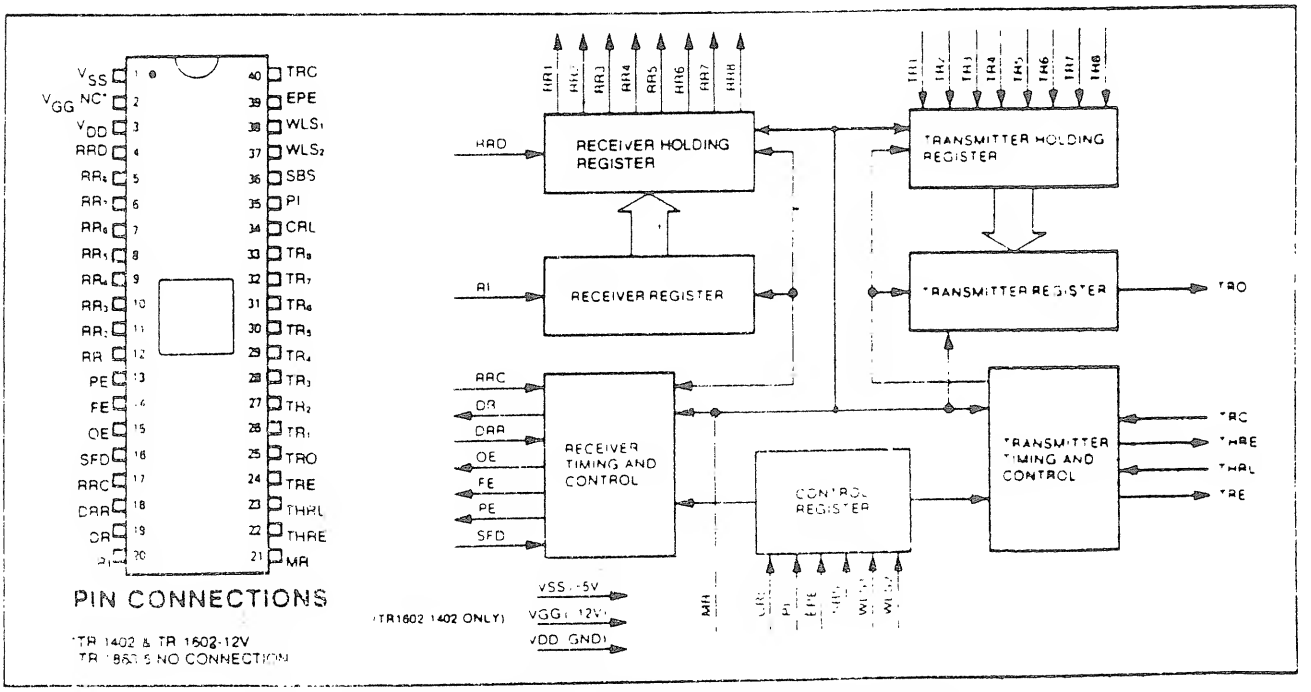
AUGUST, 1980

FEATURES

- DUAL POWER SUPPLY TR1602/TR1402
- SINGLE POWER SUPPLY — +5VDC ON TR1863/5
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  - Word Length
  - Baud Rate
  - Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  - Parity Inhibit
  - One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level for TR1602, TR1863/5)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  - Transmission Complete
  - Buffer Register Transfer Complete
  - Received Data Available
  - Parity Error
  - Framing Error
  - Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  - Receiver Register Outputs
  - Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



TR1602/TR1402/TR1863/TR1865 BLOCK DIAGRAM

GENERAL DESCRIPTION

The ASYNCHRONOUS RECEIVER TRANSMITTER is a general purpose, programmable MOS, LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start/stop bits, and optional parity. The receiver section converts a serial word with start, data, optional parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one-half when transmitting a 5 bit code. The TR1863/5 is pin- and function-compatible to the TR1402 and TR1602 except that it is −5V only and can operate up to 3.5 MHz (218.75K Baud). The standard TR1863/5 operates at 1.0 MHz (62.5K Baud). (NOTE: See TR1402A Data Sheet for operation with 5-level code-2 stop bits.)

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	VSS	-5 volts supply
2	V_{GG} — TR1602/TR1402 NC — TR1863/5	V_{GG} NC	-12 volts supply No Connection (open)
3	V_{DD} POWER SUPPLY	GND	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR8RR1 data outputs (pins 5-12)
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}
13	PARITY ERROR	PE	A high level output voltage V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16)
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16)
15	OVERRUN ERROR	OE	A high-level output voltage V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16)
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected

PIN NUMBER	NAME	SYMBOL	FUNCTION
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times times the desired receiver shift rate.
18	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the Transmitter and Receiver Holding Registers, the Transmitter Register, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REIGSTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage. V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage VOH, to a low-level output voltage, V_{OL}.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_2 and WLS_2), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.

PIN NUMBER	NAME	SYMBOL	FUNCTION
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS) This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit The TR1602 and TR1863 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WORD LENGTH SELECT	WLS_2 -WLS_1	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.

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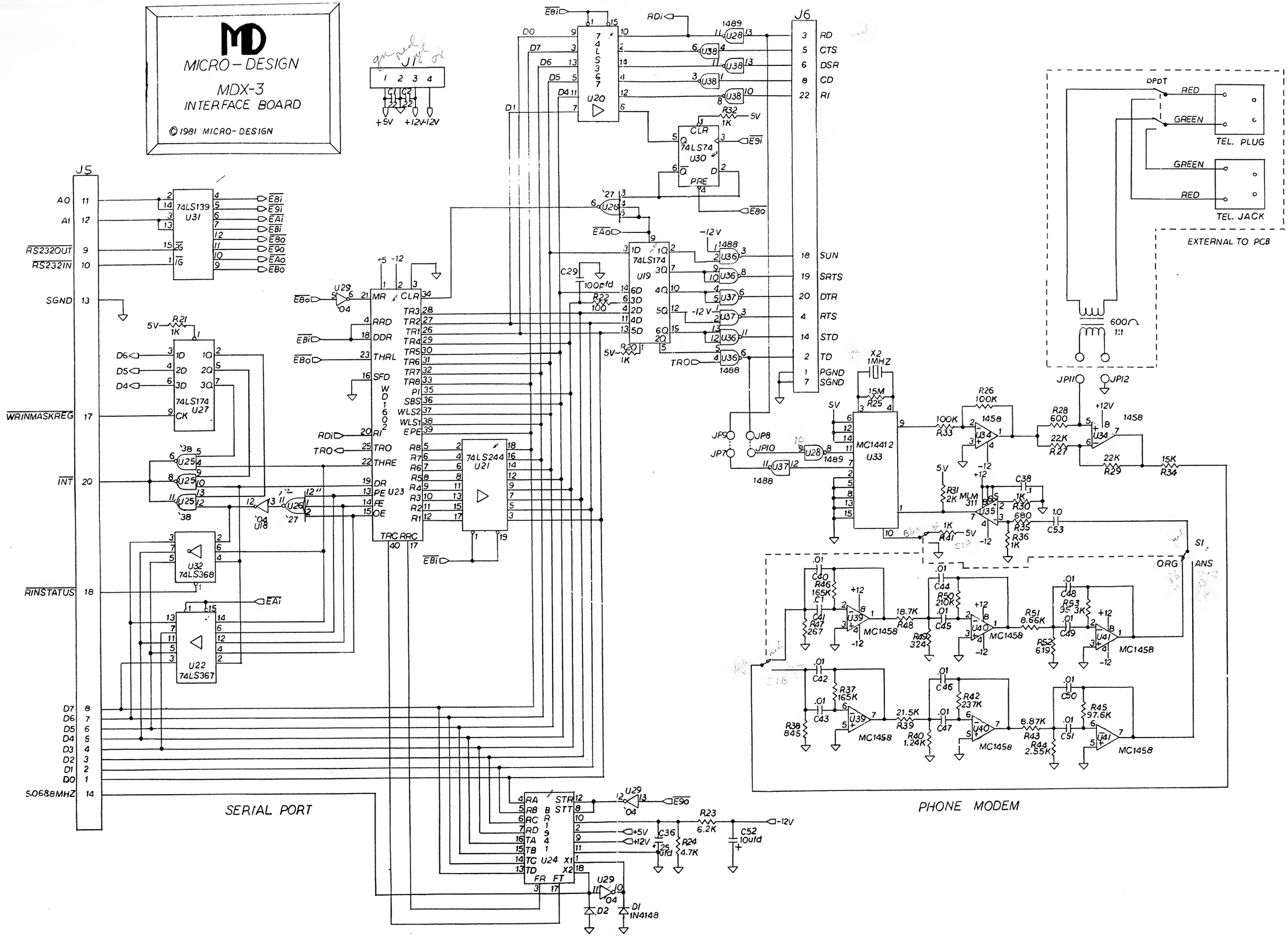
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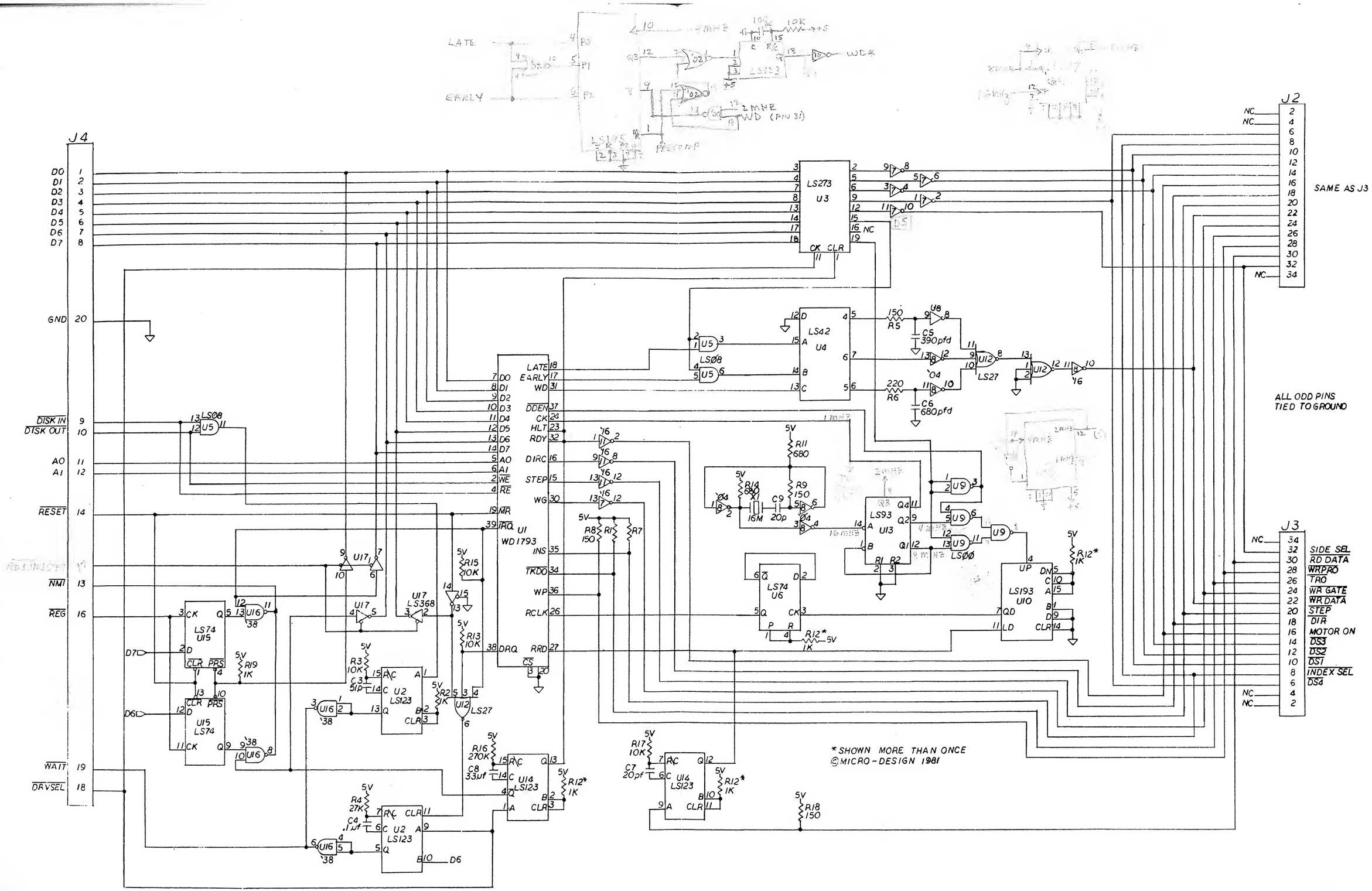
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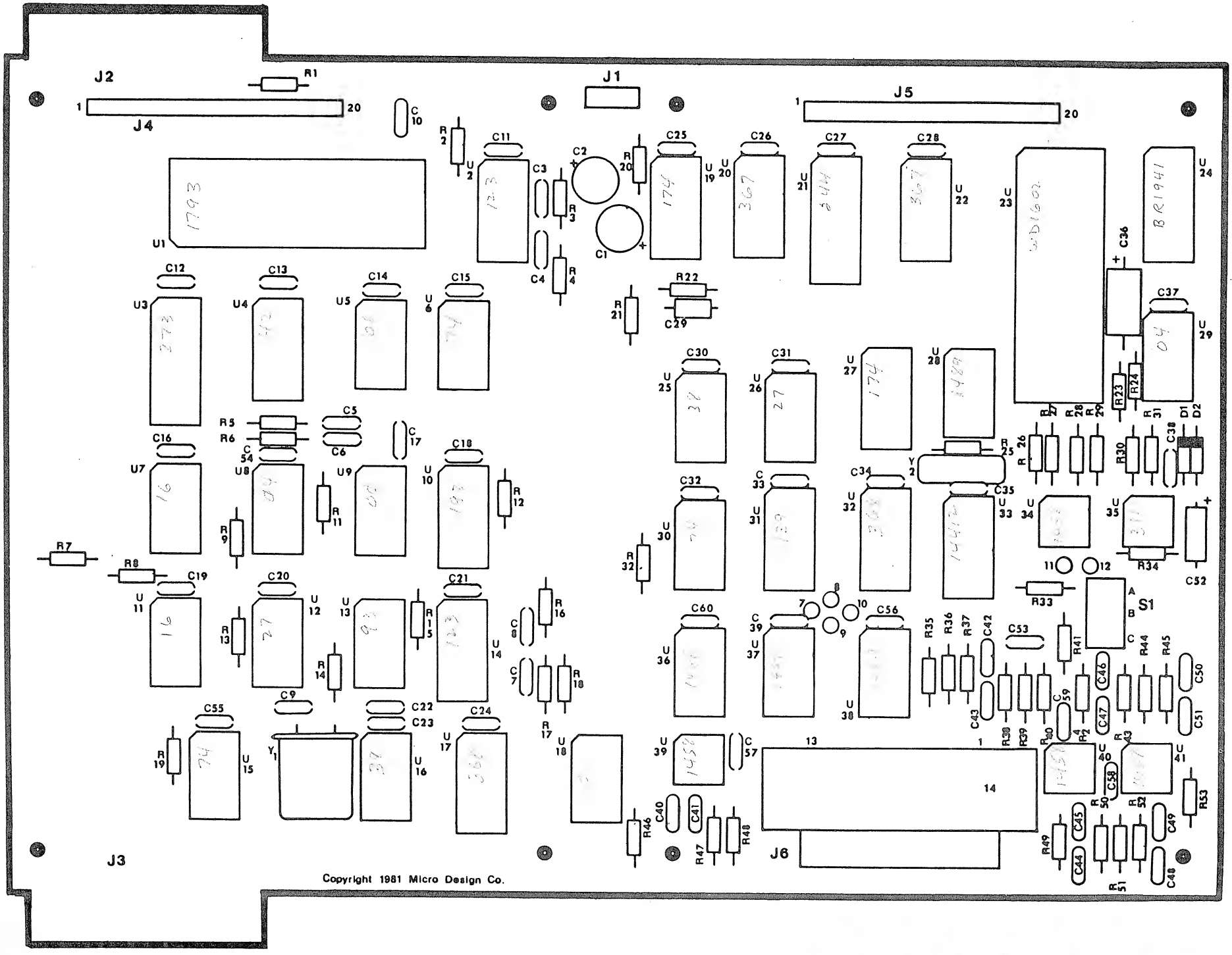
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